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L15	L13 and 19	0	<u>L15</u>
L14	L13 and 18	12	<u>L14</u>
L13	L12 and 13	29	<u>L13</u>
L12	fill\$4 near4 buffer\$1	19940	<u>L12</u>

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L11	17 and 19	2	<u>L11</u>
L10	17 and 18	49	<u>L10</u>
L9	(711/123-125)![CCLS]	549	<u>L9</u>
L8	(712/2-300)[CCLS]	10947	<u>L8</u>

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L7	L6 and 13	74	<u>L7</u>
L6	L5 and buffer\$5	8826	<u>L6</u>
L5	instruction\$1 near4 cache\$1	14168	<u>L5</u>

<u>L4</u>	L2 near8 (select\$7 or multiplex\$5 or mux or sel) near15 (configur\$6)	16	<u>L4</u>
<u>L3</u>	L2 near8 (select\$7 or multiplex\$5 or mux or sel)	515	<u>L3</u>
<u>L2</u>	(map\$6 ) near6 instruction\$1	7845	<u>L2</u>
<u>L1</u>	(map\$6 ) near6 instruciton\$1	0	<u>L1</u>

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Article Information

**IEE CNF** IEE Conference Proceeding**1. Using cache mechanisms to exploit nonrefreshing DRAMs for on-chip memories**

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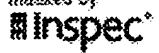
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